and no new matter has been added. The amendments are made to clarify the claims and are not intended to limit the scope of equivalents to which any claim element may be entitled.

Applicant respectfully requests reconsideration and allowance of all claims pending in the application in view of the amendments above and the remarks that follow.

The amended claims find support in the specification, for example, on page 9, lines 15-23, and Figures 2A, 3.

First §103 Rejection of the Claims

Claims 10, 11, 13-18, 20-24, 26-27, 29-38, 44 and 45 were rejected under 35 USC § 103(a) as being unpatentable over Austin (US 5,982,690) in view of Chung (US 5,442,209). Applicant respectfully traverses these grounds for rejection for the following reasons.

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also submits that the Austin patent in view of Chung is distinguishable from the present invention.

The rejection states in relevant part:

> Thus, figure 1D *(Austin)* shows all limitations of the claim *(claim 10)* except for the pair of MOSFETs is a dual gated MOSFET. However, Chung teaches in figure 1 a MOS transistor comprising a single drain, a single source and plurality of gates. This MOSFET having a function as plurality of transistors connected in parallel. The advantage of Chung's MOSFET is the chip area can be reduced in device fabrication. Therefore, it would have been obvious to one having ordinary skill in the art to make Austin's pair MOSFET (153 and 154) as a transistor having a single drain, single source, and two gates (dual gated MOSFET) for the purpose of saving space. (Italicized parentheticals added)

Claim 10, as amended, recites: "a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each amplifier, the pair of input transmission lines directly coupling the another gate in each amplifier

external to the latch circuit."

In contrast, Austin is related to a differential sense amplifier system, DSAS 100, having a first sense amplifier stage, FSAS 103,and a second sense amplifier, SSAS 105, where the two sense amplifiers act as one. *See, Austin, column 4, lines 50-57 and Figure 1D.* With respect to Austin, the Office Action states "a pair of transmission lines (outputs of circuit 103), wherein each of one of the pair of input transmission lines is coupled to another gate of the pair MOSFETs in each amplifier." The "outputs of circuit 103" are internal connections to DSAS 100. Applicant submits that outputs of circiut 103 are not transmission lines external to DSAS 100. Clearly, Austin is related to a two stage sense amplifier where the input transmission lines or bit lines such as BIT 101 and BIT 102 are external to DSAS 100, which input to FSAS 103, and are not coupled to the transistor pairs153, 154 in SSAS 105. The two stage sense amplifier is distinctly different from the circuit in claim 10 of the instant invention.

On the other hand, the latch circuit recited in claim 10 has a transmission line directly coupled to a gate of the dual-gate MOSFET, where the transmission line is external to the latch. Further, Applicant can not find in Austin any teaching or suggestion of "a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each amplifier, the pair of input transmission lines directly coupling the another gate in each amplifier external to the latch circuit," as recited in claim 10.

Chung is relied upon in the Office Action to disclose a dual-gate transistor and does not cure the deficiencies of Austin with regard to the configuration of the two stage sense amplifier lacking direct coupling of the transmission lines in FSAS 103 to the gates in SSAS 105. Thus, Applicant submits that the combination of Austin and Chung does not teach or suggest all the elements as recited in claim 10.

Independent claims 17, 23, 29, 32, 33, 37, 44, and 45 recite similar elements as claim 10 and are patentable over Austin in view of Chung for the reasons stated above plus the elements of the claims. Claims 11 and 13-16, claims 20-22, claims 24 and 26-27, claims 30-31, claims 34-36, claim 38 are dependent on claims 10, 17, 23, 29, 33, and 37, respectively, and are patentable over Austin in view of Chung for the reasons stated above plus the elements of the claims.

Applicant respectfully requests withdrawal of these rejections to claims 10, 11, 13-18, 20-24, 26-27, 29-38, 44 and 45, and reconsideration and allowance of these claims.

Second §103 Rejection of the Claims

Claims 28 and 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al. (US 6,069,828) (previous cited) in view of Austin (US 5,982,690) (previous cited) and Chung (US 5,442,209) (previous cited).

Applicant respectfully traverses these grounds for rejection for the following reasons.

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also respectfully submits that Kaneko et al. (hereafter Kaneko) in view of the Austin patent is distinguishable from the present invention.

This Office Action rejection relies on Austin and Chung regarding the details of a sense amplifier having a dual gated MOSFET, noting that Kaneko does not disclose the details of a sense amplifier. Thus, Kaneko does not cure the deficiencies in the Austin and Chung combined references. Since independent claims 23 and 40 recite similar elements as claim 10, they are patentable over Kaneko in view Austin and Chung for the reasons stated above plus the elements of the claims. Claim 28 and claims 40-43 are dependent on claims 23 and 40, respectively, and are patentable over Kaneko in view Austin and Chung for the reasons stated above plus the elements of the claims.

Applicant respectfully requests withdrawal of these rejections to claims 28, and 40-43, and reconsideration and allowance of these claims.

Comment Regarding Rejections Based on "Design Choice"

The Office Action rejection claims 15-16, 21-22, 26-27, 30-31, and 41-42 based in part as "an obvious design expedient dependent upon particular environment of use to ensure optimum performance." The mere fact that design choices are made in an innovation does not make the design choice obvious. One would expect an obvious design choice to be selected from a relatively known set of parameters, finite or infinite in number, but nonetheless from a known

set of possibilities. A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. *In re Antonie, 559* F.2d 618, 195 USPQ 6 (CCPA 1977). *See MPEP §2144.05*

Therefore, Applicant submits that the Office Action statement "an obvious design expedient dependent upon particular environment of use to ensure optimum performance," without some reference regarding the parameters does not provide a specific reason for the rejections of claims 15-16, 21-22, 26-27, 30-31, and 41-42, and therefore the Office Action has not made a prima facie case for obviousness. Further, Applicant respectfully requests that a reference, pursuant to MPEP §2144.03, which describes these parameters related to a sense amplifier using a dual gate MOSFET.

Assertion of Pertinence

Applicant has not responded to the assertion of pertinence stated for the patents cited but not relied upon by the Office Action since these patents are not relied upon as part of the rejections in this Office Action. Applicant is expressly not admitting to any assertion of their pertinence and reserves the right to address the assertion should it form a part of some future rejection.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6913) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date 9/23/2002 By

Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box RCE, Commissioner of Patents, Washington, D.C. 20231, on this 23rd day of September, 2002.

Name Amy Moriarty

Signature

Docket No. 303.586US1
WD # 320804

Micron Ref. No. 98-0588

Clean Version of Pending Claims

DRAM SENSE AMPLIFIER FOR LOW VOLTAGES
Applicant: Leonard Forbes et al.
Serial No.: 09/320,421

Claims 10, 11, 13-18, 20-24, 26-38 and 40-45, as of August 23, 2002 (date RCE filed).

10. (Four Times Amended) A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein a drain region for the dual-gated MOSFET is coupled to a drain region of the first transistor in the same amplifier, is coupled directly to a gate of the first transistor of the first conductivity type in the other amplifier in the pair of cross-coupled amplifiers, and is coupled to a gate of the dual-gated MOSFET in the other amplifier in the pair of cross-coupled amplifiers;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each amplifier, the pair of input transmission lines directly coupling the another gate in each amplifier external to the latch circuit; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the dual-gated MOSFET.

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11. The latch circuit of claim 10, wherein the first transistor includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the dual-gated MOSFET include n-channel metal oxide semiconductor (NMOS) transistors.

13. The latch circuit of claim 10, wherein the pair of input transmission lines are bit lines and wherein the bit line capacitances are removed from the pair of output transmission lines.

14. The latch circuit of claim 13, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

15. The latch circuit of claim 10, wherein the latch circuit is coupled to a power supply voltage of less than 1.0 Volts.

16. The latch circuit of claim 10, wherein the latch circuit is able to output a full output sense voltage in less than 10 nanoseconds (ns).

17. (Twice Amended) An amplifier circuit, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein the transistor of a first conductivity type in each inverter and the a dual-gated MOSFET are coupled at a drain region in the same inverter, and wherein the drain region in each inverter is further coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gated MOSFET in the other inverter of the pair of cross-couple inverters;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each inverter respectively, the pair of

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input transmission lines directly coupling the another gate in each amplifier external to the latch circuit; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region on each one of the pair of cross-coupled inverters.

18. The amplifier circuit of claim 17, wherein the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors each driven by one of the dual gates.

20. The amplifier circuit of claim 17, wherein the pair of cross-coupled inverters comprise a sense amplifier, and wherein the sense amplifier is included in a memory circuit.

21. The amplifier circuit of claim 20, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

22. The amplifier circuit of claim 21, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

23. (Four Times Amended) A memory circuit, comprising:

a number of memory arrays;

at lease one sense amplifier, wherein the sense amplifier includes:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor

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wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region of for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters;

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a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in the number of memory arrays, and wherein each one of the complementary pair of bit lines couples to another gate of the dual-gate NMOS transistor in each inverter, the complementary pair of bit lines directly coupling the another gate in each amplifier external to the sense amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

24. The memory circuit of claim 23, wherein the memory circuit includes a folded bit line memory circuit.

26. The memory circuit of claim 23, wherein the at least one sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

27. The memory circuit of claim 23, wherein the at least one sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

28. The memory circuit of claim 23, wherein the memory circuit further includes a number of equilibration and a number of isolation transistors coupled to the complementary pair of bit lines.

29. (Four Times Amended) An electronic system, comprising:

a processor;

a memory device; and

a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the complementary pair of bit lines couples to another gate of the dual-gate NMOS transistor in each inverter, the complementary pair of bit lines directly coupling the another gate in each amplifier external to the sense

amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

30. The electronic system of claim 29, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volt.

31. The electronic system of claim 29, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

32. (Four Times Amended) An integrated circuit, comprising:

a processor;

a memory operatively coupled to the processor; and

wherein the processor and memory are formed on the same semiconductor substrate and the integrated circuit includes at least one sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, is coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate transistor in the other inverter of the pair of cross-couple inverters;

a pair of bit lines, wherein each one of the pair of bit lines is coupled to another gate of the dual-gate transistors in each inverter, the pair of bit lines directly coupling the another gate of the dual-gate transistors in each inverter external to the sense amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter.

33. (Amended) A method for forming a current sense amplifier, comprising:

cross coupling a pair of inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor is coupled to a drain region of the transistor of the first conductivity type; and

coupling external to the sense amplifier one gate of each dual-gate transistor of each inverter, wherein cross coupling the pair of inverters includes directly coupling the drain region for the transistor of the first conductivity type and the drain region for the dual-gate transistor in one inverter to a gate of the transistor of a first conductivity type and to one gate of the dual-gate transistor in the other inverter.

34. The method of claim 33, wherein cross coupling the pair of inverters includes forming the first transistor of the first conductivity type as a p-channel metal oxide semiconductor (PMOS) transistor, and forming the dual-gate transistor of a second conductivity type as an n-channel metal oxide semiconductor (NMOS) transistor.

35. The method of claim 33, wherein the method further includes coupling a bit line to another gate of the dual-gate transistor in each inverter.

36. The method of claim 33, wherein the method further includes coupling an output transmission line to the drain region for the dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter. .

37. (Four Times Amended) A method for forming a sense amplifier, comprising:

forming and cross coupling a pair of inverters, wherein forming and cross coupling each inverter includes:

forming a first transistor of a first conductivity type;

forming a dual-gate transistor of a second conductivity type, wherein forming the dual-gate transistor includes coupling the drain region for the dual-gate transistor to a drain region of the first transistor in each inverter, directly coupling the drain region for the dual-gate transistor in each inverter to a gate of the first transistor of the first conductivity type in the other inverter and to a gate of the dual-gate transistor of the second conductivity type in the other inverter;

coupling a bit line to another gate of the dual-gate transistor in each inverter, each bit line directly coupling the another gate of the dual-gate transistors in each inverter external to the sense amplifier; and

coupling an output transmission line to the drain region of the first transistor and to the drain region of the dual-gate transistor in each inverter.

38. The method of claim 37, wherein forming the first transistor of a first conductivity type includes forming a p-channel metal oxide semiconductor (PMOS) transistor, and wherein forming the dual-gate transistor of a second conductivity type includes forming an n-channel metal oxide semiconductor (NMOS) transistor.

40. (Amended) A method for operating a sense amplifier, comprising:

equilibrating a first and second bit line, wherein the first bit line is coupled to a first gate of a dual-gate transistor in a first inverter in the sense amplifier and the second bit lines is coupled to a first gate of a dual-gate transistor in a second inverter in the sense amplifier, the first bit line directly coupling the first gate of the dual-gate transistor in the first inverter external to the sense amplifier and the second bit line directly coupling the first gate of the dual-gate transistor in the second inverter external to the sense amplifier;

discharging a memory cell onto the first bit line, wherein discharging a memory cell onto the first bit line drives a signal from a drain region for the first inverter directly to a gate of a PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

providing a feedback from a drain region for the second inverter to a gate of a PMOS transistor and a second gate of a dual-gate transistor in the first inverter.

41. The method of claim 40, wherein operating the sense amplifier includes operating the sense amplifier with a power supply voltage of less that 1.0 Volts.

42. The method of claim 40, wherein operating the sense amplifier includes latching an output sense signal in less than 10 nanoseconds (ns).

43. The method of claim 40, wherein the method further includes removing the bit line capacitance from a pair of output nodes of the sense amplifier.

44. (Amended) A method for operating a sense amplifier, comprising:

providing a first bit line signal directly from the external of the sense amplifier to a first gate of a dual-gate transistor in a first inverter of the sense amplifier;

providing a second bit line signal directly from the external of the sense amplifier to a

first gate of a dual-gate transistor in a second inverter of the sense amplifier

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors drives a signal directly from a drain region for the first inverter to a gate of a PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors isolates the bit line capacitances from a first and second output node on the sense amplifier.

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45. (Amended) A method for operating a sense amplifier, comprising:

providing an input signal from a bit line directly from the external of the sense amplifier to a first gate of a dual-gate transistor in a first inverter of the sense amplifier

wherein providing the input signal from the bit line to the first gate of the dual-gate transistor in the first inverter of the sense amplifier drives a signal directly from a drain region for the first inverter to a gate of a PMOS transistor and to a gate of a dual-gate transistor in a second inverter; and

wherein providing the input signal to the first gate of the dual-gate transistor isolates the bit line capacitance from an output node on the sense amplifier.